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[International papers]

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2. "Shifting Clock Jitter and Phase Interval for Impulse-Radar-Based Breast Cancer Detection," A. Toya, M.Sugawara, et. al., IEEE Biomedical Circuits and Systems Conference, 2019.
3. "A Study of Design Methodology for Mixed-Signal Circuits Using Sub-Micron Slice Structures," M. Sugawara, Doctor Thesis of Tokyo Institute of Technology, 2019
4. "Gaussian Monocycle Pulse Generator with Calibration Circuit for Breast Cancer Detection," Y. Masui, M. Sugawara, et. al., IEEE Biomedical Circuits and Systems Conference, pp. 57-60, 2018.
5. "CMOS LSI for Breast Cancer Detection," International Symposium on Biomedical Engineering, T. Imamura, M. Sugawara, et. al., 2018.
6. "Differential Equivalent Time Sampling Receiver for Breast Cancer Detection," Y. Masui, M. Sugawara, et.al., IEEE Biomedical Circuits and Systems Conference, 2017.
7. "Investigation of Phase Noise and Jitter in CMOS Sampling Clock Generation Circuits for Time-Domain Breast Cancer Detection System," A. Toya, M. Sugawara, et. al., IEEE Biomedical Circuits and Systems Conference, 2017.
8. "Physical-Weight-Based Measurement Methodology Suppressing Noise or Reducing Test Time for High-Resolution Low-Speed ADCs," M. Sugawara, et. al., IEICE Trans., Electron., Vol.E100C, No.6, 2017
9. "Synthesis and Automatic Layout of Resistive Digital-to-Analog Converter Based on Mixed-Signal Slice Cell," M. Sugawara, et. al., IEICE Trans. Fundamentals, Vol.E99-A, No.12, pp.2435-2443, 2016
10. "A 3.6 GHz Low-Noise Fractional-N Digital PLL Using SAR-ADC-Based TDC" Z.Xu, M.Sugawara et. al., IEEE JSSC, VOL. 51, NO. 10, 2016
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13. "Differential Equivalent Time Sampling Receiver for Breast Cancer Detection", Y. Masui, M. Sugawara, BIOCAS 2017(Poster) paper ID 7118
14. "Investigation of Phase Noise and Jitter in CMOS Sampling Clock Generation Circuits for Time-Domain Breast Cancer Detection System", A. Toya, M. Sugawara, et. al., BIOCAS 2017(Poster) paper ID 7274
15. "A 12b 50/70 MS/s 2.2/4.6 mW 0.03mm² CMOS SAR ADC for a frequency, performance, and power scalable ADC", S. Lee, et. al., SSDM 2013
16. "12Gb/s Duobinary Signaling with x2 Oversampled Edge Equalization", ISSCC2005 sponsored by IEEE, 3.6, Feb 2005, K. Ymaguchi, M. Sugawara et. al.
17. "3GHz 5000ppm Spread Spectrum SerDes PHY with Frequency Tracking Phase Interpolator for Serial ATA", Symposium on VLSI Circuit 2003 sponsored by IEEE, 1-7, M. Aoyama, M. Sugawara et. al.
18. "1.5GHz 5150ppm Spread Spectrum Serdes PHY with a 0.3mW, 1.5Gbps Level Detector for Serial ATA", Symposium on VLSI Circuit 2002 sponsored by IEEE, 5-3, M. Sugawara et. al.
19. "A 700Mbps BiCMOS Read Channel Integrated Circuit", ISSCC2001 sponsored by IEEE, MP12.3, Feb 2001, T. Pan, M. Sugawara et. al.
20. "A Trellis-Coded EPRML Digital Read/Write Channel IC", ISSCC99 sponsored by IEEE, MP2.2, Feb 1999, J. Chern, M. Sugawara et. al.
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26. "Expansion of Proposed Layout-Driven Mixed Signal Design Methodology to GHz

- PLL, ” M. Sugawara et. al., ECT of IEEEJ, ECT-15-030, 2015.
27. “A Proposal of novel RF power output circuit, ” M. Sugawara et. al., Analog RF study committee of IEICD, 2015
 28. “Development of Measurement Unit 24bit Audio/High-Accuracy ADC, DAC into Approximate Card-Size”, ETC of IEEEJ, ECT-14-101, 2014, M. Sugawara, et. al.
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 30. “A development of software analog by using SKILL language”, LSI and System Workshop 2014, ICD, IEICE, Mori et. al.
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 36. “A proposal of “2R-R+ segment DAC” architecture and its design methodology”, Silicon Analog RF study committee by IEICEJ,2013, M. Sugawara et. al.
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 38. “Conversion methodology from manual layout to automatic layout for analog LSI design”, LSI and System Workshop 2013, ICD, IEICE, Mori, M. Sugawara et. al.
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 40. “A proposal of 400 capacitor TEG matrix test structure with 0.1fF resolution, separated stray capacitance, by using charge based capacitance measurements (CBCM)”, ECT-13-038 by IEEEJ, 2013, M. Sugawara et. al.
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53. "Development of Signal processing ICs for LCD Color TV", Technical Report by ITEJ, TEBS97-1, pp1-6, Jun 1984, T. Sawataishi, M. Sugawara, et. al.
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